



TIME-TABLE

PG-DVLSI -AUGUST-2019 BATCH

20-10-2019 to 23-10-2019

| DATE | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|---|-------------|------------------|
| 20-10-2019 | Sunday | System Architecture (Theory) | 9.30-5.30 | Mr.Irfan Landge |
| 21-10-2019 | Monday | System Architecture (Theory) | 9.30-5.30 | Mr.Irfan Landge |
| 22-10-2019 | Tuesday | Linux and Shell Scripting (Internal Test) | 10.30-10.30 | Mr.Zubeen Sayeed |
| 23-10-2019 | Wednesday | Shell & Perl (Internal Test) | 12.00-4.00 | Mr.Zubeen Sayeed |

***Note- Lunch Break from 1.30-2.30**

Note :PG-DAC Lab is available for self - study from 6.00pm-7.30pm

Note : 24-10-2019 to 28-10-2019 Exam Preparatory Leave

Prepared by:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



| TIME-TABLE | | | | |
|------------------------------------|------------|--|---------------|------------------|
| PG-DVLSI -AUGUST-2019 BATCH | | | | |
| 14-10-2019 to 19-10-2019 | | | | |
| DATE | DAY | MODULE | TIMING | FACULTY |
| 14-10-2019 | Monday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | System Architecture (Theory) | 10.30-11.45 | Mr.Anil Vasoya |
| | | Linux and shell scripting (Theory+Lab) | 11.45-2.30 | Mr.Zubeen Sayeed |
| | | System Architecture (Theory) | 3.30-5.30 | Mr.Anil Vasoya |
| 15-10-2019 | Tuesday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | Linux and shell scripting (Theory+Lab) | 10.30-1.30 | Mr.Zubeen Sayeed |
| | | Linux and shell scripting (Theory+Lab) | 2.30-5.30 | Mr.Zubeen Sayeed |
| 16-10-2019 | Wednesday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | Linux and shell scripting (Theory+Lab) | 10.30-1.30 | Mr.Zubeen Sayeed |
| | | Linux and shell scripting (Theory+Lab) | 2.30-5.30 | Mr.Zubeen Sayeed |
| 17-10-2019 | Thursday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | Perl(Theory+Lab) | 10.30-1.30 | Mr.Zubeen Sayeed |
| | | Perl(Theory+Lab) | 2.30-5.30 | Mr.Zubeen Sayeed |
| 18-10-2019 | Friday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | Perl(Theory+Lab) | 10.30-1.30 | Mr.Zubeen Sayeed |
| | | Perl(Theory+Lab) | 2.30-5.30 | Mr.Zubeen Sayeed |
| 19-10-2019 | Saturday | PCI Design (Theory+Lab) | 8.30-10.30 | Mr.Chirag Raul |
| | | Perl(Theory+Lab) | 10.30-1.30 | Mr.Zubeen Sayeed |
| | | Perl(Theory+Lab) | 2.30-5.30 | Mr.Zubeen Sayeed |

***Note- Lunch Break from 1.30-2.30**

Note :PG-DAC Lab is available for self study from 6.00pm-7.30pm

Prepared by:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



| TIME-TABLE | | | | |
|------------------------------------|------------|--------------------------------|---------------|-------------------------|
| PG-DVLSI -AUGUST-2019 BATCH | | | | |
| 07-10-2019 to 12-10-2019 | | | | |
| DATE | DAY | MODULE | TIMING | FACULTY |
| 07-10-2019 | Monday | Effective Communication | 8.30-9.30 | Ms.Roohi Mehta |
| | | System Architecture (Theory) | 11.00-1.30 | Dr.Sangeeta Mishra |
| | | System Architecture (Practice) | 2.00-5.30 | Mr. Vaibhav Vishwakarma |
| 09-10-2019 | Wednesday | Effective Communication | 8.30-10.30 | Ms.Roohi Mehta |
| | | System Architecture (Practice) | 10.30-1.30 | Mr. Vaibhav Vishwakarma |
| | | System Architecture (Theory) | 2.00-5.00 | Dr.Sangeeta Mishra |
| 10-10-2019 | Thursday | System Architecture (Theory) | 9.30-5.30 | Dr.Sangeeta Mishra |
| 11-10-2019 | Friday | Effective Communication | 8.30-10.30 | Ms.Roohi Mehta |
| | | System Architecture (Theory) | 11.00-1.00 | Dr.Sangeeta Mishra |
| | | System Architecture (Practice) | 1.30-5.30 | Mr. Vaibhav Vishwakarma |
| 12-10-2019 | Saturday | System Architecture (Practice) | 9.30-5.30 | Mr. Vaibhav Vishwakarma |

Note : E-Library is available from 5.30-8.00pm

Note : Holiday on 08/09/2019 on account of Dassera.

Preparedby:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



TIME-TABLE

PG-DVLSI -AUGUST-2019 BATCH

30-09-2019 to 05-10-2019

| DATE | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|-------------------------------|------------|-------------------------|
| 30-09-2019 | Monday | Effective Communication | 8.30-9.30 | Ms.Roohi Mehta |
| | | Verilog HDL Internal Exam | 9.30-5.30 | Mr. Vaibhav Vishwakarma |
| 01-10-2019 | Tuesday | System Architecture (Theory) | 9.30-1.30 | Ms. Jayshree Tawade |
| | | System Architecture(Practice) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 02-09-2019 | Wednesday | System Architecture(Practice) | 9.30-5.30 | Mr. Vaibhav Vishwakarma |
| 03-09-2019 | Thursday | System Architecture (Theory) | 9.30-1.30 | Ms. Jayshree Tawade |
| | | System Architecture(Practice) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 04-10-2019 | Friday | Effective Communication | 9.30-10.30 | Ms.Roohi Mehta |
| | | System Architecture (Theory) | 9.30-1.30 | Ms. Jayshree Tawade |
| | | System Architecture(Practice) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 05-10-2019 | Saturday | System Architecture (Theory) | 9.30-1.30 | Ms. Jayshree Tawade |
| | | System Architecture (Theory) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |

Note : E-Library is available from 5.30-8.00pm

Prepared by:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



TIME-TABLE

PG-DVLSI -AUGUST-2019 BATCH

23-09-2019 to 28-09-2019

| DATE | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|-------------------------|-----------|-------------------------|
| 23-09-2019 | Monday | Verilog HDL (Theory) | 9.30-5.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 24-09-2019 | Tuesday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 25-09-2019 | Wednesday | Effective Communication | 8.30-9.30 | Ms.Roohi Mehta |
| | | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 26-09-2019 | Thursday | Effective Communication | 8.30-9.30 | Ms.Roohi Mehta |
| | | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 27-09-2019 | Friday | Effective Communication | 8.30-9.30 | Ms.Roohi Mehta |
| | | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 28-09-2019 | Saturday | Verilog HDL (Lab) | 9.30-5.30 | Mr. Vaibhav Vishwakarma |

Note : E-Library is available from 5.30-8.00pm

Note : Thakur Incubation Centre is available from 8.00-9.30pm

Prepared by:

Sd/-

Sneha More
(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra
TICA Co-ordinator



TIME-TABLE

PG-DVLSI -AUGUST-2019 BATCH

16-09-2019 to 21-09-2019

| DATE | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|----------------------|-----------|-------------------------|
| 16-09-2019 | Monday | Verilog HDL (Theory) | 9.30-5.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 17-09-2019 | Tuesday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 18-09-2019 | Wednesday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 19-09-2019 | Thursday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 20-09-2019 | Friday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 21-09-2019 | Saturday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |

Note : E-Library is available from 5.30-8.00

Prepared by:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



TIME TABLE

PG-DVLSI - AUGUST-2019 BATCH

09-09-2019 to 14-09-2019

| Date | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|----------------------|------------|-------------------------|
| 09-09-2019 | Monday | Verilog HDL (Theory) | 10.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 10-09-2019 | Tuesday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 11-09-2019 | Wednesday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 12-09-2019 | Thursday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 13-09-2019 | Friday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 14-09-2019 | Saturday | Verilog HDL (Theory) | 9.30-1.30 | Mrs.Jalpa Pandya |
| | | Verilog HDL (Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |

Prepared by:

Sd/-

Sneha More
(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra
TICA Co-ordinator



TIME TABLE

PG-DVLSI - AUGUST-2019 BATCH

03-09-2019 to 07-09-2019

| Date | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|---|-----------|-------------------------|
| 03-09-2019 | Tuesday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Sangeeta Misha |
| 04-09-2019 | Wednesday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Sangeeta Misha |
| 05-09-2019 | Thursday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Sangeeta Misha |
| 06-09-2019 | Friday | C Assignments and Praticals | 9.30-5.30 | Mr. Vaibhav Vishwakarma |
| 07-09-2019 | Saturday | Advance Digital Design(Theory) | 9.30-1.30 | Dr.Sangeeta Misha |
| | | Internal Exam (programming Fundamental) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |

Note : 02/09/2019 Ganpati Holiday

Prepared by:

Sd/-

Sneha More

(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra

TICA Co-ordinator



TIME TABLE

PG-DVLSI - AUGUST-2019 BATCH

26-08-2019 to 31-08-2019

| Date | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|---------------------------------|-----------|-------------------------|
| 26-08-2019 | Monday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Megharani Patil |
| | | Programming Fundamenta(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 27-08-2019 | Tuesday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Megharani Patil |
| | | Programming Fundamenta(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 28-08-2019 | Wednesday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Megharani Patil |
| | | Programming Fundamenta(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 29-08-2019 | Thursday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Payal Saha |
| 30-08-2019 | Friday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Payal Saha |
| 31-08-2019 | Saturday | Advance Digital Design(Theory) | 9.30-5.30 | Dr.Payal Saha |

Prepared by:

Sd/-

Sneha More
(Jr. Clerk)

Reviewed By:

Sd/-

Dr. Sangeeta Mishra
TICA Co-ordinator



TIME-TABLE

PG-DVLSI - AUGUST-2019 BATCH

19-08-2019 to 24-08-2019

| DATE | DAY | MODULE | TIMING | FACULTY |
|------------|-----------|---------------------------------|-----------|-------------------------|
| 19-08-2019 | Monday | Document Veification | 9.30-5.30 | |
| 20-08-2019 | Tuesday | Orientation | 9.30-5.30 | |
| 21-08-2019 | Wednesday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Mehgarani Patil |
| | | Programming Fundamental(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 22-08-2019 | Thursday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Mehgarani Patil |
| | | Programming Fundamental(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 23-08-2019 | Friday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Mehgarani Patil |
| | | Programming Fundamental(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |
| 24-08-2019 | Saturday | Programming Fundamental(Theory) | 9.30-1.30 | Dr.Mehgarani Patil |
| | | Programming Fundamental(Lab) | 2.30-5.30 | Mr. Vaibhav Vishwakarma |

Prepared by:
Sd/-
Sneha More
(Jr. Clerk)

Reviewed By:
Sd/-
Dr. Sangeeta Mishra
TICA Co-ordinator